Title: ROM EMBEDDED DRAM WITH DIELECTRIC REMOVAL/SHORT

IN THE CLAIMS

1. (currently amended) A method of fabricating an integrated circuit read only memory (ROM) cell comprising:

fabricating the a first conductor layer vertically above a substrate;

fabricating a dielectric layer over the first conductor layer;

fabricating a second conductor layer over the dielectric layer;

selectively removing a portion of the second conductor layer and the dielectric layer to expose the first conductor <u>layer plate</u>; and

electrically coupling the exposed first conductor to receive a program voltage.

- 2. (original) The method of claim 1 wherein the first conductor layer comprises hemispherical grained (HSG) polysilicon.
- 3. (original) The method of claim 2 wherein the hemispherical grained (HSG) polysilicon is fabricated by the method comprising:

fabricating a layer of in situ doped polysilicon; depositing undoped HSG over the layer of doped polysilicon; and applying heat to conductively dope the overlying HSG layer.

- 4. (original) The method of claim 2 wherein the hemispherical grained (HSG) polysilicon is in situ doped with arsenic.
- 5. (original) The method of claim 1 wherein the dielectric layer comprises either Ta_2O_5 or an oxide-nitride-oxide (ONO) dielectric.
- ·6. (original) The method of claim 1 wherein the second conductor layer comprises polysilicon.
- 7. (original) The method of claim 1 wherein electrically coupling the exposed first conductor comprises fabricating a third conductor layer in contact with the exposed first conductor.

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- 8. (original) The method of claim 7 wherein the third conductor layer comprises polysilicon.
- 9. (original) The method of claim 1 wherein electrically coupling the exposed first conductor comprises fabricating conductive plug in contact with the exposed first conductor.
- 10. (currently amended) A method of fabricating an integrated circuit read only memory (ROM) cell comprising:

fabricating the a first conductor layer vertically above a substrate;

fabricating a dielectric layer over the first conductor layer;

fabricating a second conductor layer over the dielectric layer;

selectively etching a portion of the second conductor layer and the dielectric layer to form a plug opening and expose the first conductor <u>layer plate</u>; and

forming a conductive plug in the plug opening to electrically couple the first conductor to receive a program voltage.

- 11. (original) The method of claim 10 wherein the first conductor layer comprises hemispherical grained (HSG) polysilicon, the dielectric layer comprises either Ta₂O₅ or an oxide-nitride-oxide (ONO) dielectric, and the second conductor layer comprises polysilicon.
- 12. (original) A method of fabricating a memory device comprising:

fabricating first and second capacitors;

removing dielectric material from the first capacitor;

coupling a storage node of the first capacitor to a voltage source node;

forming a first access transistor to couple the storage node of the first capacitor to a digit line; and

forming a second access transistor to couple the second capacitor to the digit line.

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- 13. (original) The method of claim 12 wherein coupling the storage node of the first capacitor to the voltage source node comprises fabricating a conductive plug in contact with the storage node.
- 14. (original) The method of claim 12 further comprises removing a top conductor of the first capacitor:
- 15. (original) The method of claim 14 wherein coupling the storage node of the first capacitor to the voltage source node comprises fabricating a conductive layer in contact with the storage node after the top conductor and dielectric are removed.